## REMARKS

### I. Status Summary

Claims 1-3 are pending in the present application. Claims 1 and 3 have been amended and claim 2 has been cancelled. Therefore, upon entry of this amendment, claims 1 and 3 will be pending. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the arguments set forth hereinbelow is respectfully requested.

### II. Claim Rejections Under 35 U.S.C. § 103

Claims 1-3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over EPO No. 0130381 to Auslander (hereinafter, "Auslander") in view of Mahlke et al., "A Comparison of Full and Partial Predicated Execution Support for ILP Processors" (hereinafter, "Mahlke"). This rejection is respectfully traversed in view of the above amendments and the below remarks.

Claim 1 recites a method for processing conditional jump instructions in a processor with pipeline computer architecture. Further, claim 1 recites loading and decoding a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition which specifies under which conditions the instruction is actually to be executed, and a post-condition which specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked. Claim 1 has been amended to recite that the post-condition comprises a plurality of post-condition bits that are checked in the processor. Claim 1 also recites execution of the decoded processor instruction if the

precondition is fulfilled and jumping to a jump address as a function of the relative jump distance contained in the processor instruction if the post-condition is fulfilled and the checked flag bits are set. Summarily, neither Auslander nor Mahlke, alone or in combination, teaches or suggests each and every feature as recited by amended claim 1.

Auslander is directed to a mechanism for fully executing a branch-on-any-bit-in-any-register instruction within one machine cycle of the host computing system. Means are provided whereby a branch decision may be made not only on a specified bit in the condition register, but on any bit in any of the general purpose registers provided in the system CPU. Means are also provided for saving a given configuration of the condition register in the general purpose registers for later use in subsequent branch-on-bit operations.

In the sections of Auslander cited by the Examiner, the use of a BI field is described. In particular and with reference to page 33, lines 7-13 of Auslander:

> "A bit, whose position is specified by the BI field, is selected from register RA if RA is not 0, or from the CR if RA is 0. If the bit is a 1, then the address of the next instruction is computed by the sum of the address of this instruction and the sign-extended D field. If it is a O the execution continues sequentially."

The BI field of Auslander functions as a pointer to one bit of a certain register, RA or CR (the first step). Then, it is checked if the bit of RA or CR to which the BI field points is 1 or 0 (the second step). If the bit is 1, the next instruction is computed by the sum of the address of this instruction and the sign-extended D field. Alternatively, if the bit is 0, the execution continues sequentially (the third step). As such, three steps

are needed in Auslander to decide which instruction should follow after the actual decoded instruction.

In contrast to the present invention, Auslander neither teaches nor suggests a post-condition which specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked. The inventive advantages of such a post-condition which is checked itself and which initiates the check of flag bits of an arithmetic-logic unit corresponding to the post-condition are as follows.

First, in the present invention, the post-condition itself is part of the instruction and, therefore, the processor is able to check very fast if the post-condition is fulfilled or not. In contrast, Auslander teaches a pointer to the bit which decides if a jump has to be done. According to the present invention, in the case of a non-fulfilled post-condition, only a single step is needed to decide that the execution continues sequentially. As discussed above, the teaching of Auslander disadvantageously requires three steps. As such, the claimed subject matter of the present invention has advantages in speed over the cited prior art, particularly Auslander, whereas speed is a main criterion for processors.

Second, in the present invention, after a positive check of the post-condition itself, the corresponding flag bits are checked. As a result, it is jumped to a jump address as a function of the relative jump distance contained in the processor instruction if the post-condition is fulfilled and the checked flag bits are set. Therefore, additional very complex condition settings are feasible by means of the plurality of

checked flag bits of the arithmetic-logic unit according to the claims of the present invention.

Summarily, the presently claimed subject matter comprises at least two main advantages compared to Auslander. First, a very fast detection for a sequential execution is provided if the post-condition is not fulfilled. Second, additional complex condition settings are feasible by means of the plurality of checked flag bits of the arithmetic-logic unit. Furthermore, the present invention is distinguished from Auslander by the present amendments reciting that the post-condition comprises a plurality of post-condition bits that are checked in the processor. This aspect allows even more complex condition settings to be feasible to decide if a jump has to be done dependent on the actual decoded instruction. As such, there is no teaching or suggestion in Auslander of the recited steps of the presently amended claim 1.

Mahlke fails to overcome the significant shortcomings of Auslander to teach or suggest the claimed subject matter. The Examiner stated that Mahlke teaches an additional source operand to hold a predicate specifier (precondition) and if the precondition is true, the instruction is executed, however if it is false, the instruction is not executed. (Official Action, pages 3 and 4.) However, Mahlke fails to teach or suggest a post-condition which specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked. Mahlke also fails to teach or suggest a post-condition comprising a plurality of post-condition bits that are checked in the processor as recited in the presently amended claims. Therefore, neither Auslander nor Mahlke, along or in combination, teaches or suggests a post-condition as required by claim 1. For this reason, applicant respectfully submits

that that claim 1 is not obvious in view of Auslander and Mahlke. Applicant, therefore, respectfully requests that the rejection of claim 1 under 35 U.S.C. § 103(a) be withdrawn and the claim allowed at this time.

Claim 3 recites an apparatus for processing conditional jump instructions in a processor with pipeline computer architecture. Further, claim 3 recites an instruction decoder for decoding a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition which specifies under which conditions the instruction is actually to be executed, and a post-condition which specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked. Claim 3 has been amended to recite that the post-condition comprises a plurality of post-condition bits that are checked in the processor. Claim 3 also recites that the instruction decoder is operable to check, in the case of a fulfilled precondition, whether the post-condition is fulfilled and the checked flag bits are set, if positive, driving a program counter for forming a jump address as a function of the relative jump distance contained in the processor instruction. Summarily, neither Auslander nor Mahlke, alone or in combination, teaches or suggests each and every feature recited by claim 3.

Similar to claim 1, claim 3 recites an instruction decoder for decoding a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition, and a post-condition. Further, similar to claim 1, claim 3 recites that the precondition specifies under which conditions the instruction is actually to be executed. In addition, similar to claim 1, claim 3 recites that the post-condition specifies that a conditional jump is to be processed and the corresponding flag bits of

an arithmetic logic unit are to be checked. Finally, similar to claim 1, claim 3 recites that the post-condition comprises a plurality of post-condition bits that are checked in the processor. For the reasons provided above, Auslander and Mahlke fail to teach or suggest these features. Therefore, applicant respectfully submits that claim 3 is not obvious in view of Auslander and Mahlke. Applicant, therefore, respectfully requests that the rejection of claim 3 under 35 U.S.C. § 103(a) be withdrawn and the claim allowed at this time.

## CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above amendments and remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

## DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

JENKINS, WILSON & TAYLOR, P.A.

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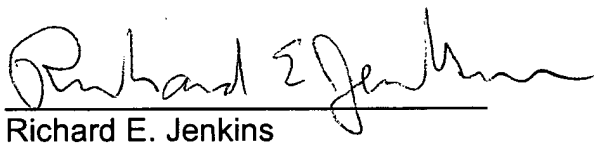
By: 

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